Trends for Mixed-Signal SoCs

- The real world signals are in analog
- Information processing and computing are in digital

Mixed Signal Problem in SoCs

The Substrate Crisis

At 0.13 micron
- Noise generation increases by 50%
- Noise sensitivity increases by 100%
**Digital Noise Coupling**

- Fast transients in digital circuits
- Switching noise in analog circuits

**Mixed-Signal IC Problem**

- Direct capacitive coupling

**Substrate Noise in a Circuitry**

- Who needs to consider the substrate coupling noise impact?

**Primary Noise Sources**

- Logic power rail bounce due to driver switching
- Chip substrate coupling
- Package resonance (excited by overtones of clock)
- Analog power rail bounce
- Noise coupling to various isolated device structures is essentially proportional to the capacitance from that device to chip substrate. No effective shielding techniques.
- Separation of noise transmitter from noise receiver makes no difference in coupled noise due to low substrate resistance
- Noise is linear with switching power on-chip
- Noise peak voltage increases as logic transitions are synchronized for a given amount of switching power. Noise energy unchanged.
- Noise energy proportional to logic power rail inductance
- Noise energy proportional to substrate (ground rail) inductance
Primary Noise Sources

- Synchronous noise
  - Using single clock for switching functions. Since the synchronous noise can excite the package system resonance in phase with the analog sampling clock its effect can be a DC shift in the sampled signal with a given noise excitation level

- Pseudosynchronous noise
  - The noise is mainly due to package resonance when excited by the CMOS switching. When the clock frequency is at the package resonant frequency the noise will increase dramatically. One must lower the Q by increasing damping

- Asynchronous noise
  - Noise from mixing clocks. This noise will start chip-package-PCB system resonating on the asynchronous clock edges. The asynchronous clocks will also couple this noise to the chip substrate and therefore to the analog circuits. Noise error can vary according to the clock phase shift

Circuit Techniques from Least to Most Noisy

- Steer current and sense current
  - current mode analog and digital

- Balanced current steering with small voltage switches
  - differential pair, differential ECL and CML

- Unbalanced current steering with large voltage switches
  - unbalanced ECL and CML

- Switch current and switch voltage (TTL)

- Concentrate current and voltage during small time intervals
  - TSPL CMOS

- Short out the supply during switching transients (CMOS)

RF IC Problem

- Weak received signals at RF input (order of microvolts)
- Several on-chip noise mechanism must be controlled
- Linear and non-linear mixing and alaising with sampling of different noise source
- Coupled noise will manifest at different frequencies (e.g. phase noise due to low frequency modulation of transistors) and analysis/simulation especially complicated. Small signal conventional) analysis may not be adequate.
- High integration will mean that both analog (like VCOs, A/D), and digital (A/D, DSP) may exists on the same chip.
Analysis of Substrate Noise in Mixed-Signal ICs

Noise: A Key Stopper in Mixed Signal Systems

Substrate Coupling: A Comprehensive View

- Substrate Coupling Circuits (Si)
- On-Chip Power/Ground Distribution Network
- Chip Package (bonding wires, package leads)
- Board-Level Power/Ground Distribution (power/ground planes, decoupling)
- Voltage Regular Module (VRM)
**Substrate Noise Injection Mechanisms**

- Capacitive injection through reverse-biased junctions
- Noise injection through contacts
- Other mechanisms
  - Parasitic capacitance between an interconnect and the substrate
  - The forward biasing of device junctions
  - Hot carriers – the high electric field between drain and source in submicron transistors
  - Ionization currents (f<100MHz) is the most important of substrate coupling sources.

**Sources of Substrate Noise:**

- Impact Ionization ($I_{\text{drain}}, V_{gs}, V_{ds}, 2mV$)
  - High electric field near the drain of saturated MOS devices

  \[
  I_{\text{impact}} = \int E_s I_d A e^{B/E(x)} dx
  \]

  Where $E_s$, $I_d$, $E(x)$ and $I_d$ are source electric field, impact ionization currents:

  Where $Es$, $Em$, $E(x)$ and $Id$ are source electric field. Constants A and B are material related coefficients.

**Substrate Noise Reception Mechanisms**

- Capacitive reception through reverse-biased junctions
- Body effect
  - Substrate noise modulates the threshold voltage of devices, e.g. NMOS transistors

  \[
  V_{\text{th}} = V_{\text{th}0} + \gamma \left( \frac{2\phi_b - V_{SB}}{\sqrt{2\phi_b}} \right) \quad \gamma = \frac{2\sqrt{qS_i N_A}}{C_{ox} \epsilon_0} \quad \phi_b = \frac{KT}{q} \ln \left( \frac{N_A}{n_i} \right)
  \]

  $V_{SB}$ - source-to-body potential, $\phi_b$ - Fermi level, $V_{th0}$ - zero bias threshold voltage, $N_A$ - the substrate doping
  - Drain voltage and drain currents of device vary linearly and as the square of the threshold voltage, respectively
  - Spikes in $V_{SB}$ result in spikes in drain voltage and current
  - In general analog circuits are much more sensitive to this effect than digital circuit
- Noise reception through contacts

**Substrate Signal Feedthrough**

- Variations in DC operating conditions
  - threshold voltages
  - junction capacitances (non-linear effect)
  - bias currents
- Variations in small signal parameters
  - gain
  - bandwidth
  - jitter/phase noise characteristics
- Signal crosstalk due to overlapping return currents through the same resistive network
- EM signal coupling to substrate for fast pulses
- One can influence to these via
  - improved physical design (layout, floorplanning, designed isolation)
  - more robust circuit topologies (e.g. converting weak analog signals to robust analog signals like in sigma-delta noise shapers)
  - improved process/package technology choices especially for isolation structures
Substrate Noise Sensor

- Illustrated circuit diagram showing a substrate noise sensor with labels such as clock, bias, diffusion capacitor, P⁺ channel stop implant, substrate contact, P⁺ bulk, and V_{\text{sensor_out}}.

Measured Substrate Noise Waveform

- An example of the substrate-noise waveform measured at the substrate noise sensor output.

- Illustration of the waveform with labeled peaks V_{\text{op}} and V_{\text{np}}.

- Mathematical expression: C_{\text{couple}} = 43.52 \text{ pF}, f_{\text{clock}} = 7.1 \text{ MHz}, t_{\text{rise/fall}} = 0.9 \text{ ns}.

External Parasitic Create Power Supply Noise

- Diagram showing bondwire, IC, package, and trace with related equations:

\[
L = 4 \text{ nH}, R = 0.01 \text{ ohm}, L_R = 4 \text{ nH}, R = 0.1 \text{ ohm},
\]

1 GHz \Rightarrow Z = 75 \text{ ohm}

Dominant Noise Source is Determined by the External Parasitic

- Graph comparing noise coupling from MOSFETs and power supply with different inductance in power supply connection.
Device Parasitics in Mixed-Signal IC Models

Substrate Current: Parasitic Return Path

Wafer and Package Parameters

Noise Coupling Mechanisms via Interconnects

- Near Field Coupling
- Substrate Coupling
- Power/Ground Crosstalk
- Signal Return Crosstalk
Practical Solutions for Substrate Noise Reduction

Chip/Package Model for Noise Analyses

Resistivity in Heavily Doped Wafer

When $d_1 = 2.5$ μm, $R_{1d} = 0$

Resistivity in Lightly Doped Wafer

Conductive or Isolating Oxide
Outline

- Wafer process level solutions
- Physical and Layout Level Solutions
- Circuit Level Solutions: Robust Circuits and Frequency Planning
- Package and Board Level Solutions: High Quality Power Distribution Network Design
- System Level Solutions: SoC versus SoP

Technology Options

- Lightly Doped Drain MOSFETs
  - Lower impact ionization currents
- SOI/Triple Well process
  - Capacitive shielding of low-frequency coupling
- Epi process with backside contact
  - Heavily-doped bulk collects noise
  - Low-impedance backplane minimizes it
  - Thin wafer for high frequency contact
- Minimize supply inductance
  - Multiple bond-wire/package pins
  - Distribute power supply pins on chip/package
  - Alternate Vdd and ground pins

Isolation Technique with Lightly-Doped

- Surface Implants
  - Channel Stop Break
  - Depletion increases with $V_{dd}$ causing well-substrate capacitance to decrease
Fabrication Process Parameters

- Process Parameters

F. Clement in J. Huijsing et al, KAP, '99

Isolation Technique with Lightly-Doped

- NMOS Transistor: Triple Well Isolation

Isolation using SOI Substrate

Physical and Layout Level Solutions
Increase Separation Distance? (Heavily Doped Substrate)

Relation between mixed-signal isolation and noise source to victim distance (heavily-doped substrate)

Lightly-Doped Substrate Isolation

- Lightly doped material
- Maximum isolation when source and victim are closer to the guard band
- Bonding inductance will affect isolation

\[
\text{Isolation} = 20 \log_{10} \frac{V_{\text{in, desired}}}{V_{\text{noise}}} \quad [dBV]
\]

Guard Rings in Lightly Doped Substrate

Relation between mixed-signal isolation and noise source to victim distance (lightly-doped substrate)
Guard Rings in Heavily Doped Substrate

Guard Ring Can be Bad

Technique for Minimize Substrate Interaction

Careful Floorplanning

- Package inductance needs to be minimized for power supplies directly connected to substrate
- Seal and pad rings affect noise transfer
- Digital signals should not
  - Be routed over or through the analog portion of the chip
  - Be routed next to sensitive lines
- The floorplan should ensure that the package pin assignments do not route sensitive analog signals near digital I/Os, supplies, or clock signals
Coupling Noise Analysis in Sigma-Delta Modulator

The modulator has a SNR=92dB when no coupling noise added.

Noise source: clock signal line.

Sensitive nodes -- shown as
1. OTA input transistors
2. Sampling capacitors

Simulation of Different Cases

Case 1. The clock is 2um away from the near NMOS. The rising/falling edge is 1ns

SNR=78 dB

Case 2. The same as case 1, expect that the clock edge is set to 0.1ns

SNR=74 dB

Case 3. The same as case 1, expect that the substrate contact is shifted to the left side (close to clock)

SNR=88 dB

Case 4. The same as case 1, expect that the clock is 12um away from the near transistors

SNR=81dB

Case 5. The same as case 1, expect that the capacitors are also taken into account, which is 5um away from the clock

SNR=66 dB

Wafer Impact Summary

- Lightly Doped
  - Isolation increase with distance with non-conductive backside
  - Backside contact with limited efficiency
  - Resistive mesh model

- Heavily Doped
  - Distance doesn’t provide isolation
  - Careful substrate grounding
  - Backside contact efficient (at high frequency?)
  - Simple model
Circuit Level Solutions:
Robust Circuits and Frequency Planning

- Low Noise Logic
  - Current steering logic (CSL, FSCL etc.)
  - Minimize switching currents in power supply

- Controlled circuit timing
  - Staggered output buffers
  - Analog sampling away from clock instants

- Fully differential analog circuitry
  - High common mode rejection
  - High power supply rejection
  - Ensure layout symmetry wrt. noise source

A Close Look to Substrate Noise Spectrum

Main peaks in substrate noise come from:
- Power/ground distribution resonance
- Circuit Switching (signal rise edge), clock

Idea:
Careful frequency planning for RF/Analog circuits in order to avoid these noise peaks.

Solutions:
- Place decoupling capacitors, change power/ground pin allocation to reduce and move the frequency of resonance
- Use differential circuits to avoid common-mode ground noise
Possible Substrate Noise Effects on an RF System

- Illustration of substrate noise effects in analog circuits. If noise falls into analog signal band, it will cause SNR reduction; otherwise, the noise in the analog circuit output.

Example: Shift Resonance Peak by Apply Decoupling

Model Used for Package Analysis

Package and Board Level Solutions

1. **Conventional Package**: TQFP or TSSOP, 5 pins for digital ground and 5 pins for analog ground, plastic modeled package with $X_{BG}$ capacitive (3.5PF).
2. **Enhanced package**: TQFP or TSSOP, 5 pins for digital ground and 5 pins for analog ground, exposed substrate contact pad for thermal management with $X_{BG}$ inductive (50pH).
Performance of LNA in Presence of Substrate Noise

\[ \text{FoM} = \frac{G \cdot IIP_3 \cdot f}{(NF - 1) \cdot P} \]

- \(G\) is the gain;
- \(IIP_3\) is the input reference third-order intercept point;
- \(NF\) is the noise figure;
- \(P\) is the power consumption;
- \(f\) is the operating frequency.

SNR = \(\frac{V_{in}}{V_{	ext{out}}^2} \)

\[ \text{SNR}_{	ext{out}} = \frac{G' \cdot V_{\text{in}}'}{G' \cdot [V_{\text{in}} + (V_{\text{in}}')^2 + V_{\text{sub}}'] + K \cdot \frac{T}{WLG} \cdot \frac{2}{3} \cdot \frac{1}{g_m} \]

\[ V_{\text{in}} = V_{\text{flicker}} + V_{\text{thermal}} + V_{\text{substrate}} \]

- \(V_{\text{flicker}}\) is flicker noise;
- \(V_{\text{thermal}}\) is thermal noise;
- \(V_{\text{substrate}}\) is the substrate noise due to mixed-signal coupling.

\[ NF = \frac{\text{SNR}_{	ext{in}}}{\text{SNR}_{	ext{out}}} = 1 + \frac{V_{\text{flicker}}}{V_{\text{in}}} + \frac{V_{\text{substrate}}}{V_{\text{in}}} \]

Comparison of Noise Power Reduction in Epitaxial and Bulk Substrates

Input Referred coupled noise power analog ground rail \((V_A)\) for conventional and enhanced packages, comparing noise levels for epitaxial and bulk substrate.

Change Switching Current Pulse Width by Applying Decoupling

Input Referred coupled noise power analog ground rail \((V_A)\) for enhanced package, comparing noise levels of switching pulse width.
### Effect of Bondwire/Package Inductance

![Graph showing the effect of bondwire/package inductance on substrate noise.](image)

- Decreasing substrate supply inductance has big impact

### Summary

- **Mixed-signal in SoC**: noisy digital circuits and sensitive analog circuits
- **Mixed-signal coupling**: noise generators, noise receivers, coupling path
- **Solutions**:
  - Wafer and process level: buried layer, triple-well …
  - Physical and layout level: guard rings, distance, floorplan …
  - Circuit level: robust circuits, frequency planning
  - Package and board level: decoupling, power distribution
  - System integration level: SoP, not SoC

### Substrate Noise Versus Package Parasitic

- **Wirebond versus Flipchip Implementation**
- Wirebond is impacted by substrate noise more seriously than Flipchip.