Distributed DVFS Using Rationally-Related Frequencies and Discrete Voltage Levels

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Abstract—As a replacement for the fast-fading Globally-Synchronous model, we have defined a flexible design style called GRLS, for Globally-Ratiochronous, Locally-Synchronous, which does not rely on global synchronization and is based on rationally-related clock frequencies derived from the same source. The design style also provides a set of supply voltages for each island to choose from. In this paper, we present the implementation details of the clock and voltage generation and distribution architecture necessary to enable Distributed DVFS. Considering a 90 nm implementation of a realistic system, we then calculate the overheads and the energy benefits compared to mesochronous and GALS approaches, quantitatively showing a considerable reduction in energy consumption compared to both solutions. Compared to GALS, the area overhead and the time necessary to change the voltage-frequency operating point are reduced several orders of magnitude.

I. INTRODUCTION

Technology scaling has made it nearly impossible to maintain global synchronism in present-day complex systems and most large and high-performance designs have adopted some form of Globally-non-Synchronous design style, where synchronous islands communicate using non-synchronous communication techniques [1], [2]. In a Globally-non-Synchronous system, the elimination of the global balanced clock tree enables significant energy improvements [3] while the latency insensitive design simplifies timing closure [1]. An additional benefit is the possibility to couple these solutions with a programmable voltage regulation system to enable Distributed (or Per-Core) Dynamic Voltage Frequency Scaling (DVFS), leading to theoretically very significant power savings [4].

A taxonomy of Globally-non-Synchronous design paradigms has been proposed in [1]. GMLS, for Globally-Mesochronous Locally-Synchronous [5] supports a single frequency and does not therefore enable DVFS. GALS [6], for Globally-Asynchronous Locally-Synchronous, is a more general technique allowing to set independently the frequency of every island, and by implication also the supply voltage. To enable DVFS, the local clocks are generated through a PLL or a programmable ring oscillator in every island, while the local supply voltages are regulated using DC-DC converters. Inter-island communication is a complex problem and carries significant complexity, performance and energy overheads [1]. Because of these reasons, the GALS approach to DVFS is suitable only for coarse-grained systems with a single-digit number of islands. Moreover, changing the voltage/frequency operating point takes several thousands of clock cycles, which makes this approach coarse-grained also in the temporal sense.

We have proposed GRLS, for Globally-Ratiochronous, Locally-Synchronous, a design style that is nearly as flexible as GALS with overheads close to the GMLS approach. In its basic form, GRLS uses multiple voltage levels and quantized clock frequencies obtained by clock division from a single source and distributed throughout the chip with an unbalanced clock tree, which enables hierarchical physical design. The schematic structure of a GRLS system is shown in Fig. 1.

Fig. 1. Schematic structure of a GRLS system

Using frequency dividers is a common industry practice for generating clock frequencies due to the simplicity of the problem of clock division. However, we innovate over existing approaches by building our local Clock Generation Units (CGUs) as clock division blocks supporting multiple input clocks to give more flexibility in the choice of the local frequencies and ultimately achieve higher energy savings through DVFS. When multiple global clocks are present, all global clocks should run at rationally-related frequencies: this can be ensured by using multiple PLLs locked on the same crystal oscillator or a single ring oscillator and multiple clock dividers in the central CGU. The GRLS approach uses quantized voltage levels by allowing every island to connect to one among a few global voltage levels, generated in a central Voltage Control Unit (VCU) by voltage regulators. Compared to the GALS approach, the area and energy overheads are significantly reduced and the time necessary to change the voltage/frequency operating point is lowered by several orders of magnitude.

The implementation details of the GRLS clock domain
crossing circuits, shown as GRLS I/F in Fig. 1 and the comparison with other state-of-the-art Globally-non-Synchronous communication interfaces has been done in [7]. The salient points of our GRLS scheme are: 1) adaptive and latency insensitive interface, 2) low latency and maximal throughput without overhead for the round-trip delay of handshake signals, 3) very low implementation overhead similar to that of mesochronous approaches and 4) good tolerance to a wide range of non-idealities.

The introduction of the GRLS approach was motivated by the need to implement an agile, distributed, low space- and time-granularity DVFS scheme. In this paper, we elaborate schemes to generate, distribute and switch among rationally-related frequencies and quantized voltage levels. We also introduce a new metric to fairly compare the energy savings that can be achieved by such schemes with other approaches, do a thorough cost-benefit analysis of our solution and quantitatively compare it to mesochronous solutions and ideal GALS systems that can always ideally switch to any arbitrary frequency and the lowest possible voltage to sustain it. Dynamically dithering between different allowed voltage/frequency points to obtain an intermediate average frequency [8] would further reduce the quantization overhead of GRLS. However, dithering is outside the scope of this paper and will be investigated in future research.

The remainder of the paper is organized as follows: we discuss related works in Section II; in Section III we present all implementation details of a GRLS system; in Section IV we calculate the energy benefits that can be obtained through DDVFS in a GRLS resource; finally, we account for overheads in a complete realistic GRLS system and show how our design style can obtain significant energy benefits compared to both GALS and GMLS approaches in Section V.

II. RELATED WORK

Rationally-related clock frequencies have been studied in Sarmenta’s work in MIT [9]. Sarmenta’s work however focuses mostly on interconnection techniques and does not take DVFS into consideration. In [7] we differentiated our approach from Sarmenta’s from a clock domain crossing point of view.

The energy benefits that can be obtained through DDVFS with a quantized voltage distribution scheme were estimated in [10]. Other research on quantized voltage levels include [11], where the design of PMOS switching circuits for a double supply-voltage system and the associated trade-offs are extensively discussed, and [12], in which a power management algorithm specifically tailored for quantized voltage levels and a discussion about the benefits of dithering with a quantized voltage distribution system can be found.

Our approach differs from these works as GRLS also proposes a realistic, quantized solution to the problem of frequency generation and we evaluate the benefits of the GRLS architecture as a whole. We also propose a metric to quantify and fairly compare the energy savings that can be obtained through the different DVFS techniques and give mathematical formulations to estimate all overheads in a GRLS system.

The article [13] also presents a complete Voltage-Frequency regulation solution based on pausable-clock GALS [14] and using two discrete voltage levels. Every island contains a stoppable programmable ring oscillator for the generation of the local frequencies. Compared to our approach, the solution proposed in [13] suffers from the drawbacks of pausable-clock GALS, namely a necessity to use complex and high-latency interfaces based on non-standard cells such as MUTEXes and impossibility to keep track of real-time because of the intrinsic unpredictability of pausable-clock systems [7]. The local ring oscillators also carry a higher overhead compared to our local Clock Generation Units while being unable to generate a crystal-quality clock frequency.

Another approach can be found in [8], where quantized voltage levels are coupled with a matched delay line and a feedback loop to generate the local frequencies. The local frequencies can have high stability but communication between the different islands is based on asynchronous FIFOs carrying a higher overhead compared to our interfaces [7]. Moreover, our solution for the generation of the local frequencies has a smaller implementation overhead and allows to change much faster the voltage/frequency operating point.

III. THE GRLS APPROACH

A. Frequency Regulation

One or more clocks running at rationally-related frequencies are generated in the central Clock Generation Unit (CGU) and distributed throughout the chip using unbalanced clock trees. The local CGUs select one among the rationally-related global clocks and divide its frequency by a programmable value to generate the local frequencies. Multiple global frequencies reduce the quantization of GRLS and can enable higher energy savings through DDVFS (Section IV). The structure of a local CGU supporting three global clock frequencies is shown in Fig. 2.

![Fig. 2. Structure of the local Clock Generation Units](image-url)
The **Selector** selects one of the input clocks \( clk_{gi} \) based on the value of the input signal \( clk_{sel} \). The structure of the selection stage ensures that, when a new clock is selected, the previously selected clock is first gated; only when all clocks are gated, the newly-selected clock is un gated. Double-stage synchronizers are used to make the system metastability-safe and glitch-free, as no assumption is made on the arrival time of the input signals. The synchronizers, however, also introduce a two-cycles latency when the global clock is changed.

The **Divider stage** divides the frequency of the selected clock \( clk_s \) by a factor \( N \). It is composed of a counter having a sequence of \( N \) states. \( init\_count \) contains the value of the counter right after it is reset and \( mid\_count \) contains the value of the counter \( \left\lceil \frac{N}{2} \right\rceil \) clock cycles later. The outputs of the comparators are used to generate the enable signals for two toggle flipflops, one positive-edge-triggered and the other negative-edge-triggered. When \( N \) is even, all edges of \( clk_t \) are synchronous with rising edges of \( clk_s \). In this situation, the negative-edge-triggered flipflop never toggles while the positive-edge-triggered flipflop toggles twice during a count sequence of the counter. When \( N \) is odd, \( clk_t \) is obtained by combining the two clocks \( clk_p \) and \( clk_n \), each running at \( \frac{N}{2} \) and in opposition of phase (Fig. 3).

![Fig. 3. Generation of \( clk_t \) with \( N = 7 \), \( init\_count = 1111 \) and \( mid\_count = 1000 \)](image)

The counter can be a simple binary counter from 0 to \( N - 1 \), in which case \( init\_count = 0 \) and \( mid\_count = \left\lceil \frac{N}{2} \right\rceil \). However, our solution consists in using an LFSR counter (Fig. 2, 3), which results in both area and power savings. An LFSR counter of \( n \) bits can be built to iterate through a sequence of up to \( 2^n - 1 \) states \( s_i \). The LFSR is designed to reset to the initial state \( s_0 = 111... \) after it reaches state \( s_{N-1} \). Therefore, \( init\_count = s_0 \) and \( mid\_count = s_{\left\lceil \frac{N}{2} \right\rceil} \). The values of \( s_{N-1} \) and \( s_{\left\lceil \frac{N}{2} \right\rceil} \) have to be pre-calculated.

We realized a CGU in Faraday fsd0j_a 90 nm technology based on the UMC 90 nm design kit. The area occupation is of a mere 140 Gate Equivalents for a CGU supporting 4 input clocks and division ratios between 1 and 15. The power consumption of the block is \( \sim 0.5mW \) when the selected clock runs at \( 1GHz \) and is only marginally influenced by the frequency of the non-selected clocks and the division ratio.

**B. Voltage Regulation**

The GRLS approach to voltage regulation consists in distributing a fixed number of supply voltages throughout the chip. The voltages are generated in a central Voltage Control Unit using a few voltage regulators. Every GRLS island is surrounded by local power rings, which are switched between the different supply voltages when needed. A schematic and a layout of the voltage switching system are shown in Fig. 4. For better area efficiency, the voltage rings can be realized in different metal layers and routed together, which eliminates the area overhead of the global voltage distribution scheme.

![Fig. 4. Voltage switching schematic](image)

The load of every resource is modeled as a variable current generator and a load capacitance, given by the capacitance of the local power grid (see Fig. 4). The PMOS switches introduce a performance penalty on the resource. The capacitance of the island power grid acts as a low-pass filter reducing the peaks of \( I_L \). The maximum voltage drop on the single PMOS transistor that is on at any time is given, in a linearized model, by \( V_{Lpeak} \), with \( g_{on} \propto \frac{W}{L} \). Using a linearized alpha-model [15], the voltage drop introduces a performance penalty that translates to a reduction of the maximal working frequency from \( f \) to

\[
\tilde{f} \left( 1 - \alpha \cdot \frac{V_{Lpeak}}{V_{TH} - V_{TH}} \right)
\]

In our reference 90 nm technology, we extracted by interpolation of the delay-voltage points (obtained from SPICE simulation) for an inverter chain \( \alpha = 1.54 \), \( V_{TH} = 0.6V \), while the conductivity \( g_{on} \) of a minimal-length PMOS transistor with a power supply of 1.2V is \( 0.469 \frac{mA}{\mu m} \). In a typical case with \( V_{TH} = 1.2V \), considering a realistic peak current of \( 40mA \) for a LEON3 RISC processor, a 2mm PMOS (which can be obtained by chaining several shorter PMOS) introduces a performance penalty of \( \sim 11\% \) and has an area occupation around \( 800\mu m^2 \), or 0.5% of the \( 400\mu m \times 400\mu m \) area of the LEON3 processor.

The time required to change the supply voltage depends on the capacitance of the local power grid and the PMOS conductivity. With \( C_L = 4pF \), which was extracted from a \( 400\mu m \times 400\mu m \) GRLS island, the switching time with a 2mm PMOS (considering the resource is stalled and does not drain any current) is less than \( 1ns \); switching between different power supplies is very fast, if not immediate, and can be done in a few clock cycles.

**IV. ENERGY ANALYSIS**

A. **Energy Components**

We model a GRLS resource as a synchronous block that needs to run at least at a frequency \( f_d \) to meet its periodic deadline constraints. If clocked at frequency \( f > f_d \), in a sufficiently long time \( T \) the resource will in average spend \( T f_d \) cycles working on its task and \( T (f - f_d) \) cycles idling. By
considering leakage constant, the energy consumption during the time \( T \) is given by:

\[
E = T \left( P_S + V^2 (f_d K_{job} + (f - f_d) K_{idle}) \right)
\]  

(1)

where \( P_S \) is the leakage power consumption, \( K_{job} \) is the average switching capacitance during the execution of the job and \( K_{idle} \) is the average switching capacitance while idling. \( K_{idle} \) is usually lower than \( K_{job} \) because the switching activity is minimized during the idle mode and can be further lowered by using clock gating techniques. However, as long as \( K_{idle} \neq 0 \), the best strategy for minimizing the power and energy consumption of the resource is to keep \( f \) as close as possible to \( f_d \).

B. Voltage-Delay Relationship

DVFS consists in lowering dynamically the voltage of the resource when a low workload is required. According to the alpha-model [15], the maximal frequency at which a system can run given the supply voltage is:

\[
f_{\text{max}}(V_{DD}) = K \left( \frac{V_{DD} - V_{TH}}{V_{DD}} \right)^{\alpha} f_H
\]

where \( \alpha \) is the velocity saturation index of the technology, \( V_{TH} \) the threshold voltage of the transistors and \( f_H = f_{\text{max}}(V_H) \) the maximal frequency at which the resource can run under the maximal power supply \( V_H \). We built a chain of 10 inverters in our reference technology to simulate a critical path. SPICE simulation using Cadence SPECTRE gave us a set of \((V, f)\) points, which we interpolated to estimate \( \alpha = 1.54 \), \( V_{TH} = 0.6 \text{V} \) and \( K = 1.19 \). The function \( f_{\text{max}}(V) \) was numerically inverted to find the function \( V_{\text{min}}(f) \) giving the minimal supply voltage that can support frequency \( f \).

Based on the technology constraints, the supply voltage can range between \( V_L = V_{TH} \) and \( V_H \). For our technology, in particular, we assume \( V_H = 2V \). The constraints on the supply voltage determine the range of operative frequencies between \( f_L = 0 \) and \( f_H = f_{\text{max}}(V_H) \), whose values depend on the critical path of the resource.

C. DVFS Scenarios

Regardless of the DVFS strategy, two constraints must always be met:

- \( f \geq f_d \) to meet the deadline constraints of the resource.
- \( V \geq V_{\text{min}}(f) \) so that the resource supports operation at frequency \( f \).

In the remainder of the paper we suppose the presence of an ideal Power Management Intelligence (PMINT) that always keeps \( f \) and \( V \) as low as possible given the constraints of the voltage and frequency regulation techniques.

For frequency regulation, we distinguish the following 3 scenarios:

- **Constant** \((f_K)\): the frequency is fixed at \( f = f_H \).
- **Ideal** \((f_I)\): the frequency can be continuously varied between \( f_L \) and \( f_H \); PMINT continuously sets \( f = f_d \).
- **Quantized** \((f_Q)\): the frequency is constrained to be a sub-multiple of one or more global frequencies \( f_g \); in this condition, PMINT sets \( f = \min(f_g) \) with \( f \geq f_d \).

Similarly, we distinguish three scenarios for voltage regulation:

- **Constant** \((V_K)\): the voltage is fixed at \( V = V_{\text{min}}(f_H) = V_H \).
- **Ideal** \((V_I)\): the voltage can be continuously varied between \( f_L \) and \( f_H \); PMINT continuously sets \( V = V_{\text{min}}(f) \).
- **Quantized** \((V_Q)\): only a discrete set of voltages \( V_g \) is allowed. PMINT always selects the minimal voltage level that can support frequency \( f \), namely \( V = \min(V_g) \) with \( V_g \geq V_{\text{min}}(f) \).

By combining all approaches for frequency and voltage regulation, 9 different DVFS scenarios can be defined. The scenarios \( f_K V_K \), \( f_K V_I \) and \( f_K V_Q \) are equivalent because the resource always runs at \( f_H \) and its power supply must be fixed to \( V_H \) regardless of the voltage constraints. We refer to the three situations simply as \( f_K \) or GMLS as the scenario corresponds to the mesochronous constraints. The \( f_I V_I \) approach approximates the behavior of an ideal GALS system with fine-grained frequency and voltage regulation. The \( f_Q V_Q \) approach corresponds to GRLS.

For comparison purposes, we consider the energy consumption of a resource under the 7 unique DVFS strategies. In order to present a significant example and without loss of generality, we consider a resource with constant switching activity \((K_{idle} = K_{job} = K)\) and negligible leakage power, common assumptions found also in [8], [12]. This simplifies equation 1 to \( E = T K V^2 f \).

D. Frequency Quantization

To rule out any influence of the voltage constraints while discussing frequency quantization, in this section we do not consider any quantized-voltage \((V_Q)\) approach. Fig. 5 shows the curves \( E(f_d) \) for the five scenarios \( f_K \) (GMLS), \( f_I V_K \), \( f_K V_I \) (GALS) and \( f_Q V_I \) with a single global frequency set at \( f_H \). The GMLS and GALS curves can be used as reference as no DVFS scenario can be worse than the first or better than the second.

Since the difference in energy consumption between the different DVFS scenarios varies widely from being nearly the same at high \( f_d \) and diverging for low \( f_d \), using the average energy consumption of the resource is a fair metric. The average energy consumption depends on the probability distribution of \( f_d \). Here and in the remainder of the paper we consider that \( f_d \) can assume any value between \( f_H \) and \( f_d \), with an uniform probability distribution. In table I, the normalized energy consumptions of the resource in the different scenarios are reported.

Note that DVFS allows a reduction of the energy consumption of the resource up to 90% when moving from the GMLS to the ideal GALS approach. Note that the quantized-frequency approaches are close to the corresponding ideal-frequency scenarios, mostly because the best energy benefits
TABLE I
NORMALIZED AVERAGE ENERGY CONSUMPTION FOR DIFFERENT DVFS SCENARIOS

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Constraints</th>
<th>Avg. Energy Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_K$ (GMLS)</td>
<td>Constant Freq.</td>
<td>100%</td>
</tr>
<tr>
<td>$f_QV_K$</td>
<td>Quantized Freq., Constant Volt.</td>
<td>46.58%</td>
</tr>
<tr>
<td>$f_QV_K$</td>
<td>Ideal Freq., Constant Volt.</td>
<td>13.10%</td>
</tr>
<tr>
<td>$f_QV_K$</td>
<td>Quantized Freq., Ideal Volt.</td>
<td>10.26%</td>
</tr>
</tbody>
</table>

The average energy consumptions for the different scenarios are reported in table III.

TABLE III
NORMALIZED AVERAGE ENERGY CONSUMPTION FOR DIFFERENT DVFS SCENARIOS

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Constraints</th>
<th>Avg. Energy Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_K$ (GMLS)</td>
<td>Constant Freq.</td>
<td>100%</td>
</tr>
<tr>
<td>$f_QV_K$</td>
<td>Quantized Freq., Constant Volt.</td>
<td>43.60%</td>
</tr>
<tr>
<td>$f_QV_K$</td>
<td>Ideal Freq., Quantized Volt.</td>
<td>10.26%</td>
</tr>
<tr>
<td>$f_QV_K$</td>
<td>Quantized Freq. and Volt.</td>
<td>10.26%</td>
</tr>
<tr>
<td>$f_QV_K$</td>
<td>Ideal Freq. and Volt.</td>
<td>10.26%</td>
</tr>
</tbody>
</table>

E. Voltage Quantization

Fig. 6 shows the energy curves for the $f_K$ (GMLS), $f_QV_K$ (GALS), $f_QV_K$, $f_QV_K$ and $f_QV_Q$ (GRLS) scenarios. Two

By exhaustive exploration it is possible, given the number of global voltages, to find which voltage values minimize the average energy consumption. In table IV are reported the minimal average energy consumptions of the resources for numbers of global voltage levels between 1 and 4. The $f_QV_K$ (GALS) and $f_QV_K$ average energy consumptions, which can be considered as $V_Q$ approaches with an infinite number of global voltages, are also reported.

The table shows that having multiple global voltages is very important for obtaining better DVFS energy savings. The introduction of two global voltages reduces the average energy consumption of the resource more than two times. Already with 2 voltage levels, the average energy consumption for the GRLS ($f_QV_Q$) approach is within 48% of the ideal $f_QV_K$; 4 supply voltages lower the figure to 14% and give an average energy consumption that is only 34% higher compared to the ideal GALS ($f_QV_K$) scenario.
V. OVERHEAD ANALYSIS

A GRLS system is made up by the collection of several resources, possibly with different structure and deadline constraints. Considering the average power overheads introduced by the frequency regulation architecture, the total power consumption of a GRLS system is given by:

\[ P = P_{\text{RES}} + P_{\text{CGU}} + P_{\text{CTR}} \]

where \( P_{\text{RES}} \) is the total power consumed by all resources, \( P_{\text{CGU}} \) is the power consumption of the local CGUs and \( P_{\text{CTR}} \) is the power consumption of the global clock trees. The power consumed by the CGU is mostly proportional to the frequency of the global clock on which the resource is locked while, if the layout is fixed, \( P_{\text{CTR}} \) is proportional to the sum of all global frequencies, as all clock trees are similar in structure and size and the dynamic power consumed in every clock tree is proportional to the frequency at which it is switching.

Let us consider a 2\text{mm} \times 2\text{mm} wide GRLS system divided in 25 400\text{um} \times 400\text{um} GRLS islands, each containing a LEON3 RISC processor. We obtain from Cadence Encounter that, when clocked at the maximum frequency of 1GHz with a 2V power supply, each LEON3 processor consumes \( \sim 20\text{mW} \). We assume that the probability distribution of \( f_d \) for every resource is uniform between 100MHz and \( f_H = 1\text{GHz} \) and that the probability distributions of different resources are uncorrelated. With these assumptions, we calculate the average power consumption of the system for different DVFS scenarios (Table V). Different GRLS scenarios are identified by the global frequencies and the number of global voltages.

VI. CONCLUSION

In conclusion, the GRLS approach has proven to be very effective for energy reduction through the use of Distributed DVFS, allowing to reduce more than 5 times the average energy consumption of a realistic, low-granularity system compared to the GMLS approach while achieving energy benefits and extreme area overhead reduction compared to a GALS approach based on PLLs and voltage regulators. Since the GRLS approach allows changing the voltage/frequency operating point much faster than GALS, dithering [8], that we plan to investigate in the near future, would further enhance its energy benefits.

REFERENCES

[3] Reference masked for blind review
[7] Reference masked for blind review