ForSyDe
Rising the abstraction level in System Design

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March 27th, 2008
1. Introduction to ForSyDe
   - The abstraction gap problem
   - What is ForSyDe?
   - Examples
   - Simplified Design Flow
   - Initial implementation of ForSyDe

2. Current ForSyDe’s implementation details
   - The compilation problem
   - Deep Embedding + Embedded compiler
   - The Sharing Problem: Observable Sharing
   - The Polymorphism Problem: Dynamic Types
   - Deep-embedding process-constructor parameters
   - Components
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The abstraction-gap problem

- Systems designed nowadays (and electronic components in particular) are increasingly complex.
- Market pressure calls for two apparently opposite constraints:
  - Efficiency ⇒ It is required to handle low-level details at design time ⇒ low abstraction level
  - Example: Large layout parts of today’s high performance processors are designed and optimized by hand.
  - Low time-to-market and complex features ⇒ It is preferable to avoid dealing with low-level details ⇒ high abstraction level
  - Example: SoC (System on Chip) architectures embed multiple heterogeneous components.
- ForSyDe’s main motivation is to solve the resulting abstraction gap problem
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- **ForSyDe (Formal System Design)** is a System Design methodology that models Systems at a high abstraction level and bridges the abstraction gap using a technique called *transformational design refinement*.

- A system in ForSyDe is modelled as a network of cooperating *processes* which are communicated via *signals*. Processes perform computations over its input signals and forward the results to adjacent processes through output signals.

- Processes are created from *process constructors*. The creation of a process entails setting the parameters (values or functions) of a process constructor. These parameters determine the behaviour of the process over its input signals.

- Communication and computation are separated. Thus, time is abstracted, allowing multiple models of computation (Synchronous, Untimed, Discrete Time and Continuous).

- To simplify this talk, a Synchronous MoC will be assumed.
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A.Acosta (KTH)
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**Signal**

- A (possibly infinite) sequence of events, where each event has a tag and a value.
- All events in a signal must have values of the same type.
- In ForSyDe, signals are modelled as lists of event values. Tags are implicitly determined by the location of the values in the list.

\[ S = \langle v_0, v_1, v_2, \cdots \rangle \]

- The interpretation of tags depends on the model of computation. (e.g. in general, identical tags in different signals don’t imply equal times)
- In the Synchronous MoC
  - the system is governed by a global clock
  - tags correspond to global-clock cycles (i.e. each value corresponds to a clock cycle).
**Key concepts (I)**

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Processes and Process Constructors

**Process**

Processes are defined as pure functions over signals.

\[ p : S \times S \times \ldots \times S \rightarrow S \times S \times \ldots \times S \]

\[ i_0 = i'_0, i_1 = i'_1, \ldots, i_n = i'_n \Rightarrow p(i_1, i_2, \ldots, i_n) = p(i'_1, i'_2, \ldots, i'_n) \]

**Process constructor**

Creates a processes out of:

- Values: process configuration parameter or initial state.
- Functions: process behaviour.
- Note: These functions operate over the values carried by signals, not over signals themselves.

\[ p = pc(v_1, v_2, \ldots, f_1, f_2, \ldots) \]
Key concepts (II)
Processes and Process Constructors

- **Process**

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- **Process constructor**

  Creates a processes out of:
  \[ \begin{array}{cccc}
  v_1 & v_2 & \cdots \\
  f_1 & f_2 & \cdots 
  \end{array} \]
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**Primitive Process-Constructor Examples**

- mapSY primitive process-constructor

  \[
  \text{mapSY}(f) = \langle f(v_0), f(v_1), f(v_2), \ldots \rangle
  \]

- delaySY\(_k\) primitive process constructor

  \[
  \text{delaySY}_k = \langle s_0, s_0, s_0, \ldots, v_0, v_1, v_2, \ldots \rangle
  \]
Primitive Process-Constructor Examples

- mapSY primitive process-constructor

\[ \text{mapSY}(f) \quad \langle v_0, v_1, v_2, \cdots \rangle = \langle f(v_0), f(v_1), f(v_2), \cdots \rangle \]

- delaySY\_k primitive process constructor

\[ \text{delaySY}_k(s_0) \quad \langle v_0, v_1, v_2, \cdots \rangle = \langle s_0, s_0, s_0, \cdots, v_0, v_1, v_2, \cdots \rangle \]
The \textit{sourceSY} derived process constructor

\[
\text{sourceSY}(f, s_0) = \ll s_0, f(s_0), f(f(s_0)), f(f(f(s_0))), \cdots \gg
\]

Sample use of a process constructor: the trivial \textit{plus1} process

\[
\text{plus1} = \text{mapSY}(+1)
\]
More Examples

- The `sourceSY` derived process constructor

\[ sourceSY(f, s_0) = \langle s_0, f(s_0), f(f(s_0)), f(f(f(s_0))), \ldots \rangle \]

- Sample use of a process constructor: the trivial `plus1` process

\[ plus1 = mapSY(1) \]
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Simplified Design Flow

0
Specification Model

1
Implementation Model

2
Implementation (e.g. VHDL)
0) The designer creates the **specification model** as a network of processes.

\[
\begin{align*}
\vec{i_1} & \rightarrow P_1 \rightarrow \vec{s_1} \rightarrow P_2 \rightarrow \vec{o_1} \\
\vec{i_2} & \rightarrow P_3 \rightarrow \vec{s_2} \rightarrow \vec{o_2}
\end{align*}
\]
1) **Transformational refinement**

- The **specification model** is transformed into a lower-level **implementation model**.
- This stage is in charge of bridging the abstraction gap using transformation rules.
- Rules can be:
  - semantic preserving (automatic)
  - non-semantic preserving (require interaction with the designer).
- Relies on the formal foundations of ForSyDe.
- Theoretically designed but not yet implemented.
2) Implementation Mapping

- Transforms the implementation model into an architecture-specific implementation
  - Software: C, C++ . . .
  - Hardware: VHDL, SystemC, Verilog . . .
  - Special cases: Simulation, Verification.
- Current lack of automatization of (1) entails working with the specification model directly
- Implemented mappings: Simulation, VHDL (in progress)
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The specification models were initially expressed in a **shallow** Haskell-embedded DSL (*Domain Specific Language*).

A DSL, as opposed to a general purpose programming language (C, C++, Ada, Haskell) is designed for a specific task. Examples: YACC, Postscript, GraphViz, VHDL ...

An Embedded DSL is implemented inside a general purpose programming language (called host language), as a library.

The embedding can be shallow or deep:

- **Shallow**: The data structures supporting the embedded language only reflect semantics.
- **Deep**: The data structures supporting the embedded language reflect the structure of the program which created them.

The embedded approach has some advantages and disadvantages:

- The host language plus all its surrounding machinery (compilers, libraries ..) can be reused.
- The syntax and semantics of the two languages (embedded and host) might differ.
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Initial implementation of ForSyDe (I)

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- A DSL, as opposed to a general purpose programming language (C, C++, Ada, Haskell) is designed for a specific task.
  - Examples: YACC, Postscript, GraphViz, VHDL ...
- An Embedded DSL is implemented inside a general purpose programming language (called host language), as a library.
- The embedding can be shallow or deep
  - Shallow: The data structures supporting the embedded language only reflect semantics.
  - Deep: The data structures supporting the embedded language reflect the structure of the program which created them.
- The embedded approach has some advantages and disadvantages
  - The host language plus all its surrounding machinery (compilers, libraries ..) can be reused.
  - The syntax and semantics of the two languages (embedded and host) might differ.
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Initial implementation of ForSyDe (II)

Why Haskell?

- Strongly-typed: DSLs are easy to embed.
- Lazy: infinite data structures are natively supported.
  - Signals can be easily shallow-embedded with a type isomorphic to lists.

```
data Signal a = NullS | a :- Signal a
```

- Purely functional with higher-order functions:
  - Process constructors are just pure, higher-order functions after all.

```
mapSY :: (a -> b) -> Signal a -> Signal b
mapSY _ NullS = NullS
mapSY f (x:-xs) = f x :- (mapSY f xs)
```

- Haskell is particularly good for creating function combinators, useful to create process connection patterns.
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   - The abstraction gap problem
   - What is ForSyDe?
   - Examples
   - Simplified Design Flow
   - Initial implementation of ForSyDe

2. Current ForSyDe’s implementation details
   - The compilation problem
   - Deep Embedding + Embedded compiler
   - The Sharing Problem: Observable Sharing
   - The Polymorphism Problem: Dynamic Types
   - Deep-embedding process-constructor parameters
   - Components
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The compilation problem

- The initial **shallow** embedding only allows simulating the models (The Signal type is not aware of how the system was built).
- We want to be able to implement the transformational refinement and implementation mapping stages without losing the ability of simulating our models.

**Alternatives**
- Standalone Haskell compiler: excessive and unfeasible given our development resources.
- Creating a backend for an existing compiler: slightly less excessive and unfeasible.
- Keep the shallow embedding for simulation and use a static analyzer for compilation: very difficult without restricting how the host language is used.
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Deep Embedding + Embedded compiler

- Goal: Create a new deep-embedded Signal, aware of of the system structure.
  - The new Signal will be the intermediate representation of an embedded compiler, in charge of the implementation mapping.

- A possible simplified solution (for a structural hardware design language).

```haskell
data Signal = Comp String [Signal]
inv, latch :: Signal -> Signal -- sample primitives
inv s = Comp "inv" [b] -- inverter primitive
latch s = Comp "latch" [s] -- latch primitive
toggle :: Signal -- sample circuit
toggle = let o = inv (latch o) in o
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- Problems:
  - Detecting sharing between components (there is no way to detect the loop in `toggle`).
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The Sharing Problem: Observable Sharing

- Explicit tagging: the designer provides a unique label for each component.

```haskell

type Label = String
data Signal = Comp Label String [Signal]
toggle = let o = inv "tinv" (latch "tlatch" o) in o
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- Artificial tag syntax, uniqueness is not guaranteed.
- Transform `Signal` into a monad which generates unique labels.
  - Guaranteed uniqueness but inconvenient monadic syntax.
- Observable sharing: link components through unmutable references

```haskell

data Ref a = Ref (IORef a) deriving Eq
newRef = Ref.unsafePerformIO.newIORef
data Signal = Comp String [Ref Signal]
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- Pros: Guaranteed uniqueness without inconvenient syntax
- Cons: Impure extension
  - However, referential transparency will be preserved if sharing is (all known Haskell compilers are based in graph reduction).
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So far we have solved the sharing problem, but how to take polymorphism in account?

```haskell
-- phantom parameter to ensure type-consistency
data Signal a = Signal PrimSignal
-- first attempt, incorrect
data PrimSignal = MapSY (a->b) (Ref PrimSignal) ...
mapSY :: (a->b) -> Signal a -> Signal b
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Solution: Dynamic types.

```haskell
class Typeable a where
  typeOf :: a -> TypeRep
toDyn :: Typeable a => a -> Dynamic
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-- correct
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Deep-embedding process-constructor parameters

- The value of the process constructor parameters is not enough, the compiler needs their AST for later translation.
- Solution: Template Haskell (compile-time metaprogramming extension)

```haskell
[d| decs |] :: Q [Dec] -- lift the AST of the enclosed declarations
$(exp) -- splice declarations or expressions
-- exp must be a Haskell expression of type (Q Exp) or (Q [Dec])

-- the Dynamic value is kept for simulation
data PrimSignal = MapSY Dynamic [Dec] (Ref PrimSignal) ...
mapSY :: (Typeable a, Typeable b) =>
        ProcFun (a->b) -> Signal a -> Signal b
newProcFun :: Q [Dec] -> Q Exp
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- Example: `plus1`

```haskell
plus1 :: (Typeable a, Num a) => Signal a -> Signal a
plus1 = mapSY (+1)
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plus1 :: (Typeable a, Num a) => Signal a -> Signal a
plus1 = mapSY p1
    where p1 = $(newProcFun [d| doPlus1 :: Num a => a -> a |
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- Similarly to HDLs like VHDL, ForSyDe has support for hierarchical design through components.
- Let’s see a simple example. Design a serial adder using components in 5 simple steps.
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- Let’s see a simple example. Design a serial adder using components in 5 simple steps.

1) Create a process function which adds one to its input

```haskell
addOneF :: ProcFun (Int32 -> Int32)
addOneF = $(newProcFun [d| addOneF :: Int32 -> Int32
addOneF n = n + 1 |])
```
Components

Similarly to HDLs like VHDL, ForSyDe has support for hierarchical design through components.

Let’s see a simple example. Design a serial adder using components in 5 simple steps.

1. Define the components for the adder:

   \[
   \text{in1} :: \text{Signal Int} \\
   \text{AddFour} \leftarrow \text{mapSY} (+1) \rightarrow \text{mapSY} (+1) \rightarrow \text{mapSY} (+1) \rightarrow \text{mapSY} (+1) \\
   \text{out1} :: \text{Signal Int}
   \]

2) Create a system function corresponding to the unit adder

   \[
   \text{addOneProc} :: \text{Signal Int32} \rightarrow \text{Signal Int32} \\
   \text{addOneProc} = \text{mapSY} \text{ addOnef}
   \]
Similarly to HDLs like VHDL, ForSyDe has support for hierarchical design through components.

Let’s see a simple example. Design a serial adder using components in 5 simple steps.

3) Subsystem definition associated to the unit adder

```haskell
addOneSysDef :: SysDef (Signal Int32 -> Signal Int32)
addOneSysDef = $(newSysDef 'addOneProc ["in1"] ["out1"])
```
Components

- Similarly to HDLs like VHDL, ForSyDe has support for hierarchical design through components.
- Let’s see a simple example. Design a serial adder using components in 5 simple steps.

4) Create the main system function

```haskell
addFour :: Signal Int32 -> Signal Int32
addFour = $(instantiate "addOne3" 'addOneSysDef) .
  $(instantiate "addOne2" 'addOneSysDef) .
  $(instantiate "addOne1" 'addOneSysDef) .
  $(instantiate "addOne0" 'addOneSysDef)
```
Components

- Similarly to HDLs like VHDL, ForSyDe has support for hierarchical design through components.
- Let’s see a simple example. Design a serial adder using components in 5 simple steps.

5) Finally, build the main system definition

```plaintext
addFourSys :: SysDef (Signal Int32 -> Signal Int32)
addFourSys = $(newSysDef 'addFour ["in1"] ["out1"])
```
Create process functions
(newProcFun)

ProcFun (a1 -> .. -> an)

Create system function
(possibly using process constructors i.e. mapSY etc)

sysF :: Signal i1 -> Signal i2 -> ...
   Signal in ->
       (Signal o1, Signal o2, .. Signal om)

∀n, m ∈ N ∪ {0}

Create System Definition
(newSysDef)

sysDef :: SysDef (Signal i1 -> Signal i2 -> ...
   Signal in ->
       (Signal o1, Signal o2, .. Signal om))

∀n, m ∈ N ∪ {0}

Create an instance
(instantiate)

Backends
(simulate etc)
Further Reading

Ingo Sander.  

Alfonso Acosta.  

Koen Claessen and David Sands.  
Observable Sharing for functional circuit description.  

John T. O’Donnell.  
Embedding a Hardware Description Language in Template Haskell.  